Amendments to the Specification:

Please replace the title of this application with the following amended title:

Computer System Employing Pipeline Operation.

Please replace the paragraph beginning on page 8, line 35 with the following amended paragraph:

Next, when the period "c" starts, the decoded signal of the instruction 1 is stored into the decode signal register 5, and the data processing between specified operand data is executed by the EXB 7 according to the decoded signal of the instruction 1 outputted from the decode signal register 5. Instruction 1 is executed as an execution stage in the pipeline in the high frequency ALU 20, and the execution result of the instruction 1 is obtained as the output 23 of the ALU 20, and the low frequency ALU in charge is selected. The decode register valid signal DRCRV becomes effective from the period "c", and signal DRVFST indicating the initial cycle of DECRV becomes effective. In the period "c", the enable signal 38 becomes high and the data and the control signal for executing the instruction 1 are inputted to the latches 8, 9, and 10. In this example, in the period "c", the ALU 21 is selected, the ~~ALU21~~ALU 21 executes an operation during two machine cycles, and then the output 24 is obtained. In addition, the instruction 3 is fetched in the IFB 1 and the instruction 2 is decoded in the DECB 4 in the period "c".

Please replace the paragraph beginning on page 9, line 11 with the following amended paragraph.

Next, when the period "d" starts, the execution result processed according to the instruction 1 is stored in the EX register 30, and the instruction 2 is operated in the EXB 7. First of all, the high frequency ALU 20 executes the instruction 2 as the pipeline execution stage, the execution result of the instruction 2 is obtained as the output 23 of the ALU 20, and the low frequency ALU selected as the low frequency ALU in charge for executing the instruction 2 in the period "c" is switched from the ALU 21 to the ALU 22. The output of the selector 26 and the output of the ALU 20 are inputted to the selector 28, and the output of the selector 26 is selected only in case the mismatching signal 34 is high and inputted to the register 30. The enable signal 38 turns to be low level by DRVFST, and data and a control signal for executing the instruction

1 are kept in the latches 8, 9, and 10. On the other hand, in the period "d", the enable signal 39 turns to be high level, and data and a control signal for executing the instruction 2 are kept in the latches 11, 12, 13. Thus, the ALU 21 executes the instruction 1 for the period of "d" as well as the period of "c". As a result, the instruction 1 is executed during two cycles of period "c" and period "d". The ALU 22 begins the execution of the instruction 2 for the period of "d", and the execution result of the instruction 2 is obtained as the output 25. As described as follows, the ALU 22 executes the instruction 2 during the period of "e". As a result, the instruction 2 is executed during two cycles of period "d" and period "e". In addition, the verification processing and the output processing of the execution result of the instruction 1 are operated for the period of "d". First of all, EXRV indicating the effectiveness of the EX register 30 becomes high, and the EXRV is inputted into the comparator 32. When the EXRV is high and the data in the EX register 30 and the output of the low frequency ALU selected by the selector 26 match, the matching signal 33 becomes high level. If these does not match, the mismatching signal 34 becomes a high level. In the period of "d", the enable signal 39 is high level, the output of the ALU 21 is selected by the selector 26, and then the output of the ALU 21 and the output of the register 30 are compared by the comparator 32. The execution result of the instruction 1 by the high frequency ALU 20 in one machine cycle and the execution result of the instruction 1 by the low frequency ALU 21 in two machine cycles are compared. In this example, the instruction 1 is finished within the basic machine cycle, so the output of the register 30 and the output of the ~~ALU21~~ALU 21 matches, so the correct operation in the ALU 20 is confirmed and the matching signal 33 becomes high, and the output of the register 30 (this is the execution result of the instruction 1 executed by the high frequency ALU 20 in one machine cycle) becomes the output of the ~~EXB7~~EXB 7 of the pipeline execution stage. Thus, the instruction 1 can be executed by the pipeline processing correctly at the high frequency. In addition, the instruction 4 is fetched in the IFB 1 and the instruction 3 is decoded in the DECB 4 in the period "d".

Please replace the paragraph beginning on page 10, line 17 with the following amended paragraph:

In the period of "e", the execution result executed according the instruction 2 is stored in the EX register 30, and the instruction 3 is executed in the ~~EXB7~~EXB 7. In the following description, the description in the same part as the period of "c" is roughly described. First of all,

the instruction 3 is executed as an execution stage in the pipeline in the high frequency ALU 20, and the execution result "3" of the instruction 3 is obtained as the output 23 of the ALU 20. While, the low frequency ALU in charge of the instruction 3 is switched from the ~~ALU22~~ALU 22, which is currently selected in the period of "d", to the ALU 21. In the period of "e", the enable signal 38 turns to be high according to the high level of the matching signal 33 in the previous cycle. According to the enable signal, data and the control signal to execute the instruction 3 are inputted to the latches 8, 9, and 10. On the other hand, the enable signal 39 is low in the period of "e", and data and the control signal to execute the instruction 2 are kept in the latches 11, 12 and 13. Thus, the ~~ALU22~~ALU 22 executes the instruction 1 for the period of "e" as well as the period of "d". As a result, the instruction 2 is executed during two cycles of period "d" and period "e". The ~~ALU21~~ALU 21 begins the execution of the instruction 3 for the period of "e", and the execution result "3" of the instruction 3 is obtained as the output 25 at the first 1 machine cycle. As described as follows, the ~~ALU21~~ALU 21 executes the instruction 3 and obtains the correct execution result "3" at the next period of "f", which is the second machine cycle for execution of the instruction 3. In addition, as the verification processing and the output processing of the execution result of the instruction 2 for the period of "e", the output of the ALU 22 and the output of the register 30 are compared by the comparator 32 because the enable signal 39 is low and the output of the ALU 22 is selected by the selector 26. In this example, the instruction 2 is finished within the basic machine cycle, so the matching signal 33 becomes high, and the output of the register 30 (this is the execution result of the instruction 2 executed by the high frequency ALU 20 in one machine cycle) becomes the output of the EXB7 of the pipeline execution stage.